

IN THE ABSTRACT

Please replace the Abstract with the following:

A-In a method for testing a testable electronic device having a first and a second plurality of test arrangements, e.g. scan chains, is disclosed. A first shift register (110) is used in parallel with a second shift register (130) to time-multiplex a first test vector (102) and a second test vector (104) into a number of smaller test vectors (102a-c; 104a-c) for provision to the first and second plurality of test arrangements. By varying the size of the first shift register (110) and the second shift register (130) a trade-off between the number of pins of the electronic device to be contacted and the required test time can be made. Preferably, The first shift register (110) is may be coupled to a first buffer register (120) and second shift register (130) is may be coupled to a second buffer register (140) for enhanced test data stability. First shift register (110) and second shift register (130) can be partitions of a larger shift register, e.g. a boundary scan chain. The method can also be used in a reverse way by time-demultiplexing test result vectors into a single vector at the output side of the testable electronic device.